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Z86319

PS/2 MOUSE CONTROLLER

FEATURES

Device	ROM (KB)	RAM* (Bytes)	I/O Lines	Voltage Range
Z86319	2	125	13	4.5V to 5.5V

Note: *General-Purpose (144K Total RAM)

- 0°C to + 40°C Operating Temperature Range
- Low-Power Consumption: 25 mW (Typical)
- P24-P27 Can Be Configured with a Voltage Divider During Input Mode
- On-Chip Oscillator (Tolerance = ±10%)
- Fast Instruction Pointer: 1.5 µs @ 4 MHz
- ESD Protection Circuitry
- Hardwired Watch-Dog Timer (WDT)
- Excellent System Level EMI/EFT/ESD

GENERAL DESCRIPTION

The Z86319 is a member of the Z8 family of CMOS microcontrollers architecture to be used in mouse applications. These devices offer on-board pull-up and pull-down resistors, a trip-point buffer to accommodate opto-transistor outputs, and high drive ports capable of up to 10 mA current sinking per pin (3 pins maximum).

A permanently enabled Watch-Dog Timer ensures operational reliability across a broad range of mouse application environments. The precision RC oscillator filters out high-frequency noise from the oscillator input pin. When configured as inputs, P24-P27 have built in voltage dividers (25K pull-up /7.5K pull-down). The input levels are designed for connection to the emitters of the opto-transistors and switch at a voltage level of 0.4 V_{DD}.

For applications requiring powerful I/O capabilities, the Z86319 provides dedicated input and output lines that are grouped into three ports. There are two basic address spaces available to support this configuration: Program Memory, and 125 bytes of general-purpose registers.

The Z86319 device provides two on-chip 8-bit programmable counter/timers with a large number of user-selectable modes. Each counter/timer is driven by its own 6-bit programmable prescaler. The Z86319 counter/timers off-load system real-time tasks such as counting/timing and input/output data communications for increased system efficiency.

GENERAL DESCRIPTION (Continued)

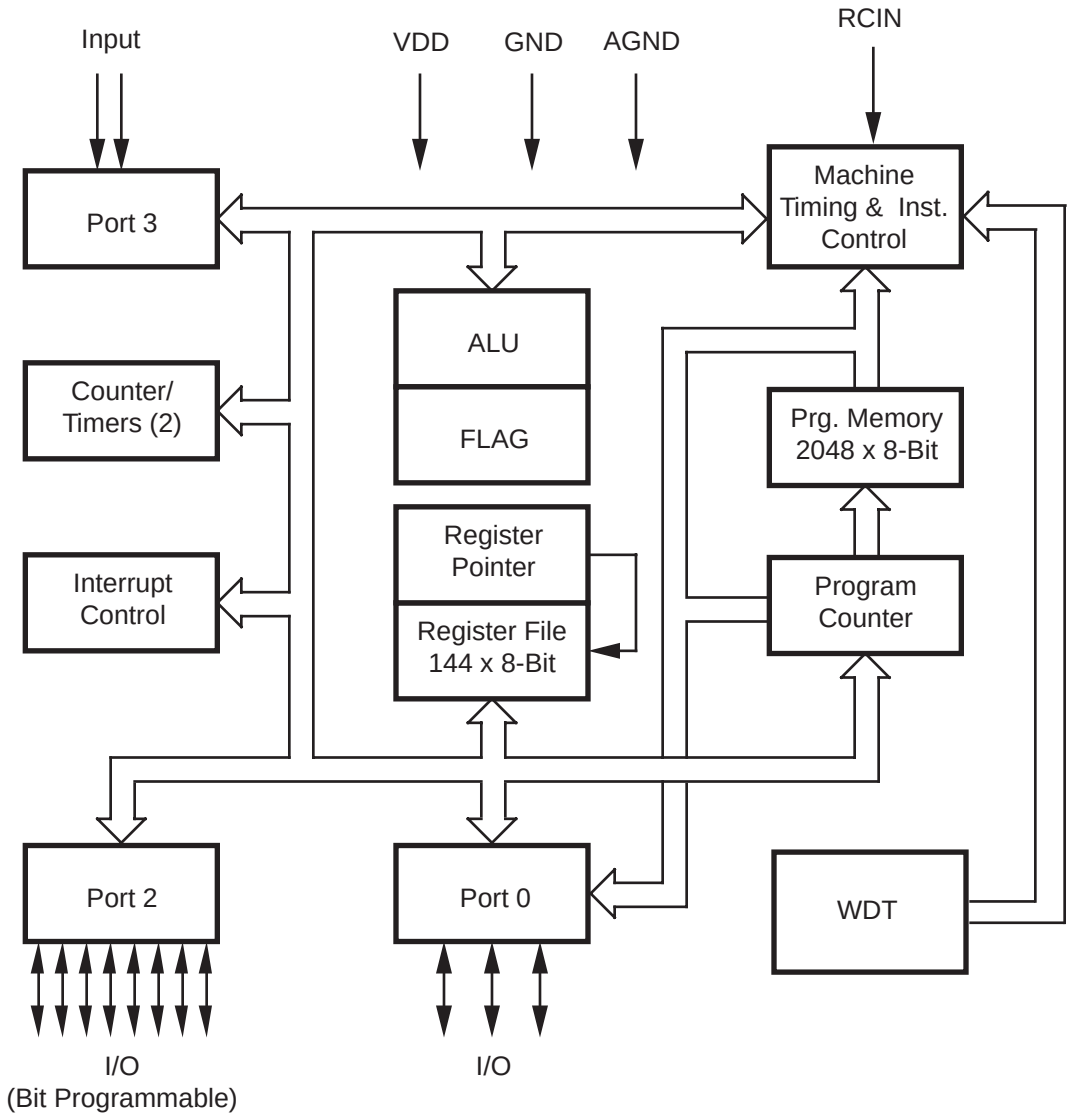


Figure 1. Z86319 Functional Block Diagram

PIN DESCRIPTIONS

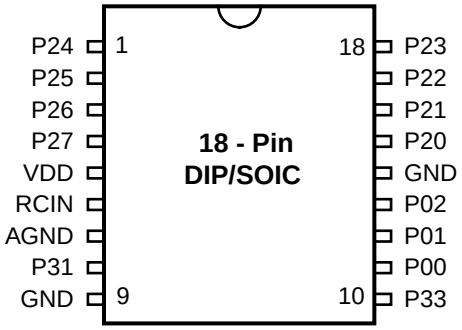


Figure 2. 18-Pin DIP/SOIC Pin Configuration

Table 1. 18-Pin DIP/SOIC Pin Identification

Pin #	Symbol	Function	Direction
1-4	P24-P27	Port 2, Pins 4,5,6,7	In/Output
5	V_{DD}	Power Supply	Power
6	RCIN	RC Oscillator	Input
7	AGND	Analog Ground	Ground
8	P31	Port 3, Pin 1	Input
9	GND	Ground	Input
10	P33	Port 3, Pin 3,	Input
11-13	P00-P02	Port 0, Pins 0,1,2	In/Output
14	GND	Ground	Ground
15-18	P20-P23	Port 2, Pins 0,1,2,3	In/Output

PIN FUNCTIONS

RCIN. A precision 1% resistor is connected to RCIN, generating oscillation with an internal capacitor.

Resistor values and corresponding typical frequencies are shown in Table 2 and graph chart (Figure 3).

Table 2. Resistor Values and Corresponding Typical Frequencies

External Resistor	Average Frequency
14.0K	5.01 MHz
15.0K	4.70 MHz
16.0K	4.43 MHz
17.0K	4.19 MHz
18.0K	3.97 MHz
19.0K	3.78 MHz
20.0K	3.60 MHz
21.0K	3.44 MHz
22.0K	3.30 MHz
23.0K	3.16 MHz

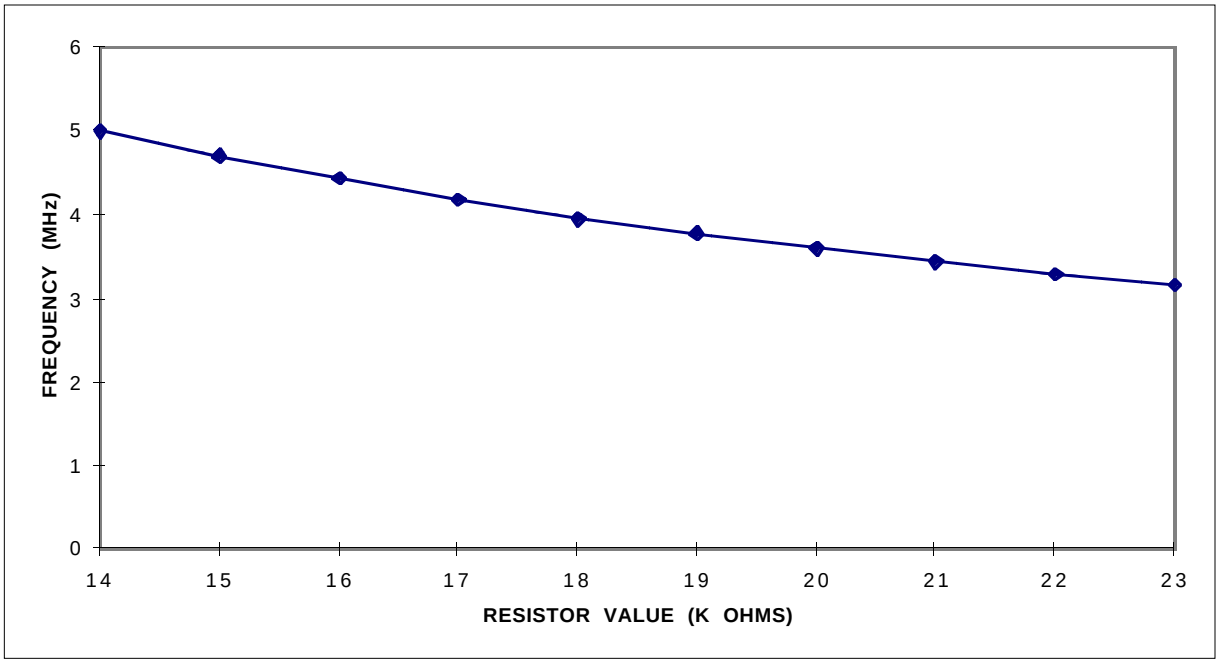


Figure 3. Z86319 RC Frequency in Function of the External Resistance (typical numbers)

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 4).

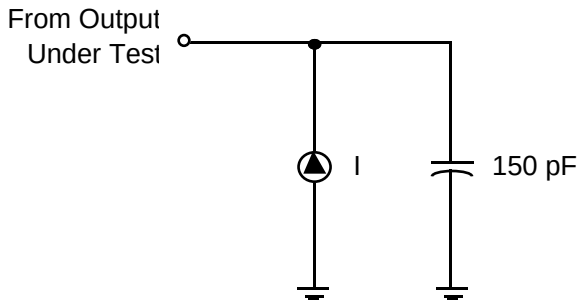


Figure 4. Test Load Diagram

ABSOLUTE MAXIMUM RATINGS

Sym	Parameter	Min	Max	Units
V_{DD}	Supply Voltage*	–0.3	+7	V
T_{STG}	Storage Temp	–65°	+150°	C
T_A	Oper Ambient Temp	0°	40°	C

Notes:
*Voltages on all pins with respect to Ground.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This rating is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAPACITANCE

T_A = GND = 0V, f = 1.0 MHz, unmeasured pins returned to Ground.

Parameter	Min	Max
Input Capacitance	0	10 pF
Output Capacitance	0	20 pF
I/O Capacitance	0	25 pF

V_{CC} SPECIFICATION

V_{CC} = 4.5V to 5.5V

Using the precision RC oscillator feature, f = 4.0 MHz ±10% under the following conditions:

- V_{CC} = 5.0V ±10%
- Temp 0 to 40°C
- Application board capacitance:
  - 2.0 pF max.
  - 0.5 pF min.

DC ELECTRICAL CHARACTERISTICS

$4.5V \geq V_{DD} \leq 5.5V$

		T_A = 0°C to +40°C			
Sym	**Parameter**	**Min**	**Max**	**Units**	**Conditions**
V_{IH}	Rising Input Schmitt-Triggered	2.3	3.2	V	Note 1
V_{IL}	Falling Input Schmitt-Triggered	1.3	2.2	V	Note 1
V_{IL}	Input Low Voltage CMOS Input			V	
V_{OH}	Output High Voltage	V_{DD} – 0.4		V	I_{OH} = –2.0 mA; V_{DD}=4.5V
V_{OL1}	Output Low Voltage		0.4	V	I_{OL} = +4.0 mA; V_{DD}=5.5V
V_{OL2}	Output Low Voltage		0.8	V	I_{OL} = 10.0 mA, 3 Pin Max; V_{DD}=5.5V
V_{LV}	V_{CC} Low Voltage Protection	2.25	2.95	V	@ 4 MHz Max, Note 2
V_{TP}	Trip Point Voltage (P24-P27)	1.9	2.5	V	P24-P27; V_{DD}=5.5V
		1.5	2.1	V	V_{DD}=4.5V
I_{IL}	Input Leakage	–1.0	1.0	µA	V_{IN} = 0V, or V_{CC} Note 4
I_{OL}	Output Leakage	–1.0	1.0	µA	V_{IN} = 0V, or V_{CC} Note 4
I_{DD}	Supply Current		4.5	mA	@ 4 MHz, Note 3; V_{DD}=5.5V
I_{DD1}	Standby Current		2.2	mA	@ 4 MHz, Note 3; V_{DD}=5.5V
I_{PU}	Pull-Up Current (100K)	–20		µA	V_{IH} @ 1V
	P00-02, P31, P33		–95	µA	V_{IH} @ 1V
I_{PD}	Pull-Down Current (100K)	+20		µA	V_{IL} @ 3V
	P00-02, P31, P33		+85	µA	V_{IL} @ 4V
I_{PU}	Pull-Up Current (10K)	–370		µA	V_{IL} = 0V
	P20, P22		–670	µA	V_{IL} = 0V

Notes:

1. The min. and max. values of the Schmitt-Trigger input voltages track each other over temperature, V_{DD}, and process variations.
2. The device is functional from V_{DD} down to V_{LV} voltage. The minimum operational V_{DD} is determined by the value of the V_{LV} voltage at ambient temperature. The V_{LV} voltage increases as the temperature decreases.
3. All input pins are tied to GND and all output pins are floating.

AC ELECTRICAL CHARACTERISTICS

Timing Diagrams

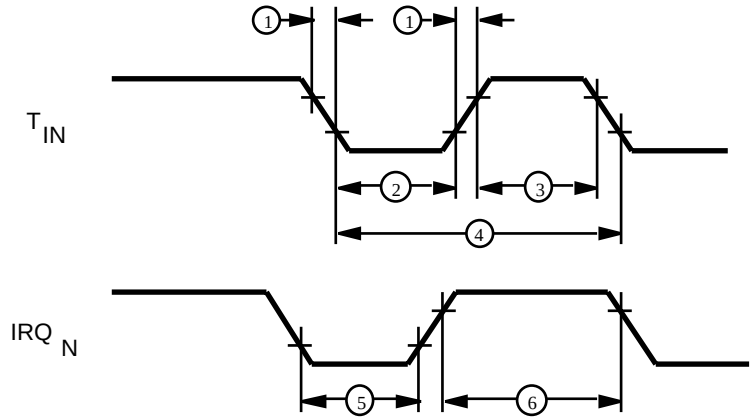


Figure 5. Electrical Timing Diagram

				T_A = 0°C to +40°C			
No	**Symbol**	**Parameter**	**V_{DD}**	**Min**	**Max**	**Units**	**Notes**
1	TrTin, TtTin	Timer Input Rise and Fall Time	5.5V		100	ns	1
2	TwTinL	Timer Input Low Width	5.5V	70		ns	1
3	TwTinH	Timer Input High Width	5.5V	2.5TpC			1
4	TpTin	Timer Input Period	5.5V	4TpC			1
5	TwIL	Int. Request Input Low Time	5.5V	70		ns	1,2
6	TwIH	Int. Request Input High Time	5.5V	2.5TpC			1,2
	Twdt	Watch-Dog Timer Time Out	5.5V	10		ms	
	TPOR	Power-On Reset Time	5.5V	2	10	ms	
	TpC	RC Oscillator Clock Period	5.5V	220	5000	ns	

Notes:

1. Timing Reference uses 0.9 V_{DD} for a logic 1 and 0.1 V_{DD} for a logic 0.
2. Interrupt request through Port 3 (P33-P31)

PIN FUNCTIONS

Port 0 (P02-P00). Port 0 is a 3-bit, I/O programmable, bi-directional, CMOS-compatible I/O port. These three I/O lines can be configured under software control to be input or output (Figure6). When Port 0 is configured as an input port, all lines have the capability to either sink or source (ROM mask selectable) current emulating a 100K pull-down or pull-up resistor. Port 00-02 can be accessed through the P0 register (register address 00). The upper 5 bits of this 8-bit register always reads “11111.” Writing to the upper 5 bits has no effect (see Figure 34). The lower 3 bits of the P0 register are read/write. Current versus pin voltage graphs are shown in Figures 7 and 8.

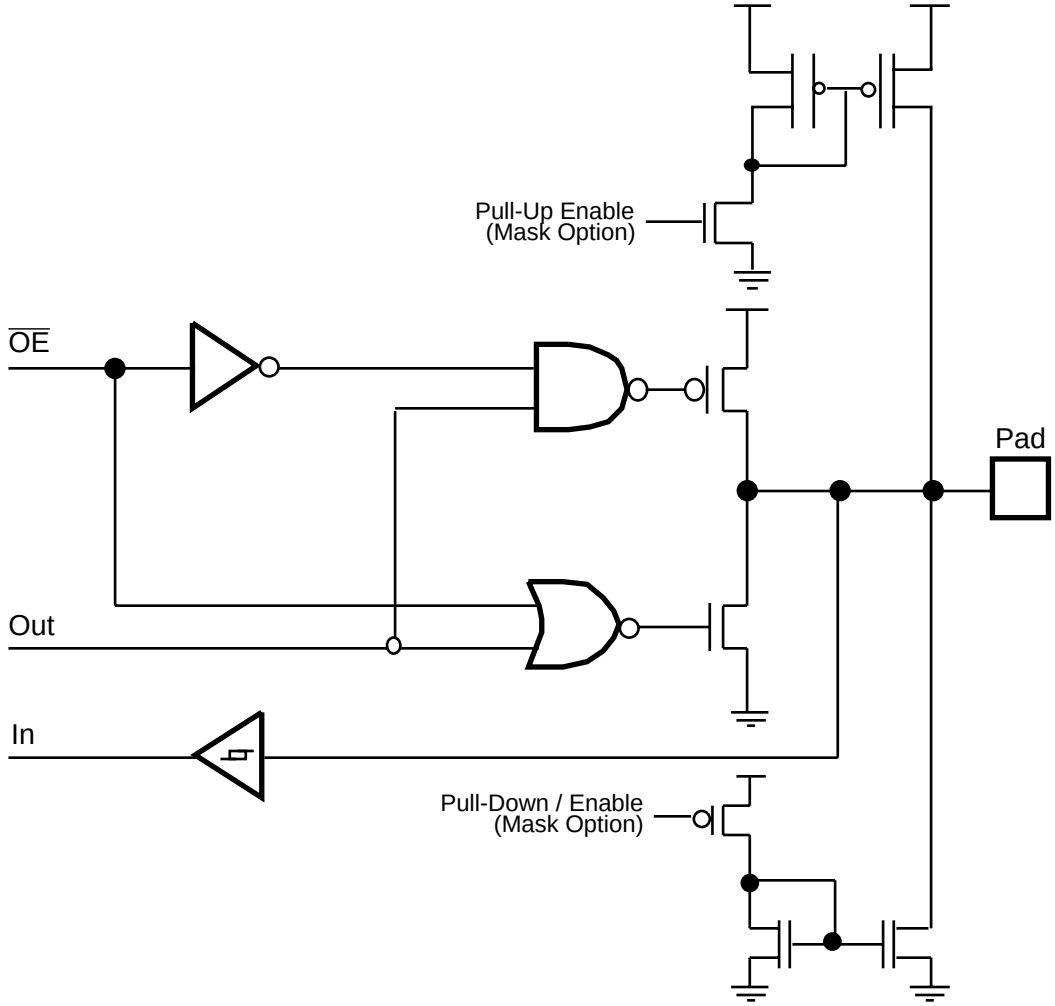


Figure 6. Port 0 Configuration

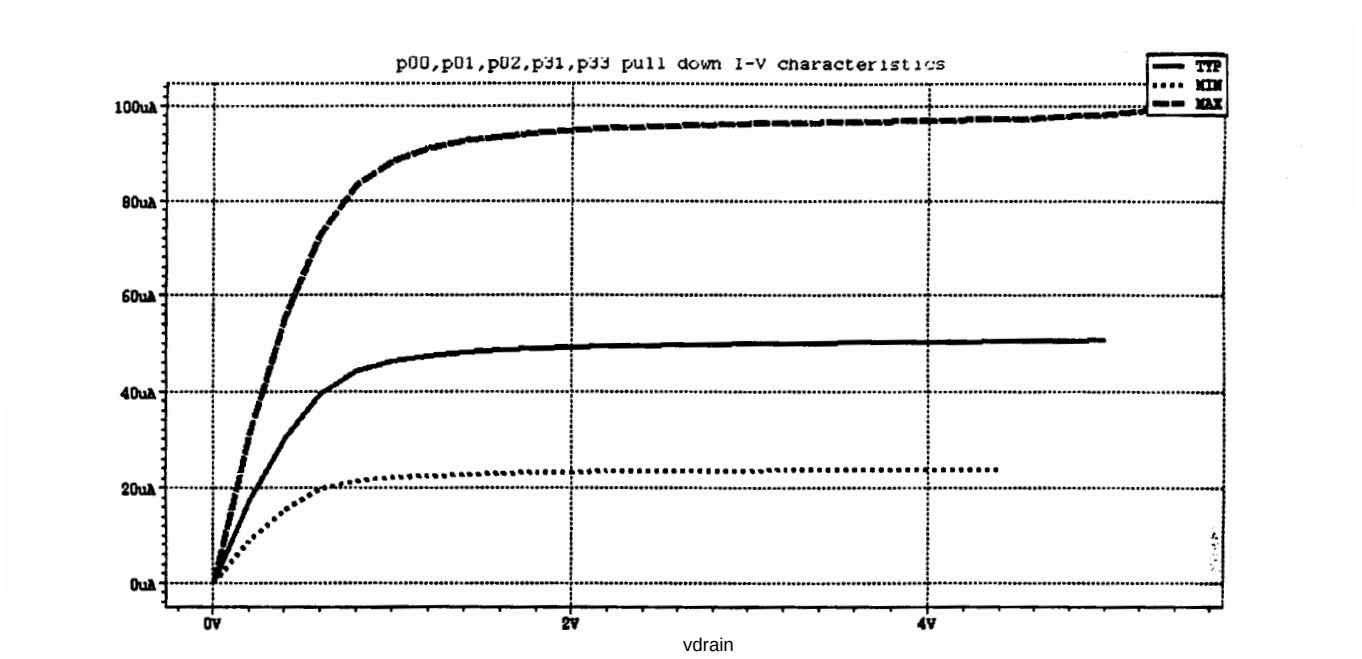


Figure 7. Current vs Pin Voltage Values

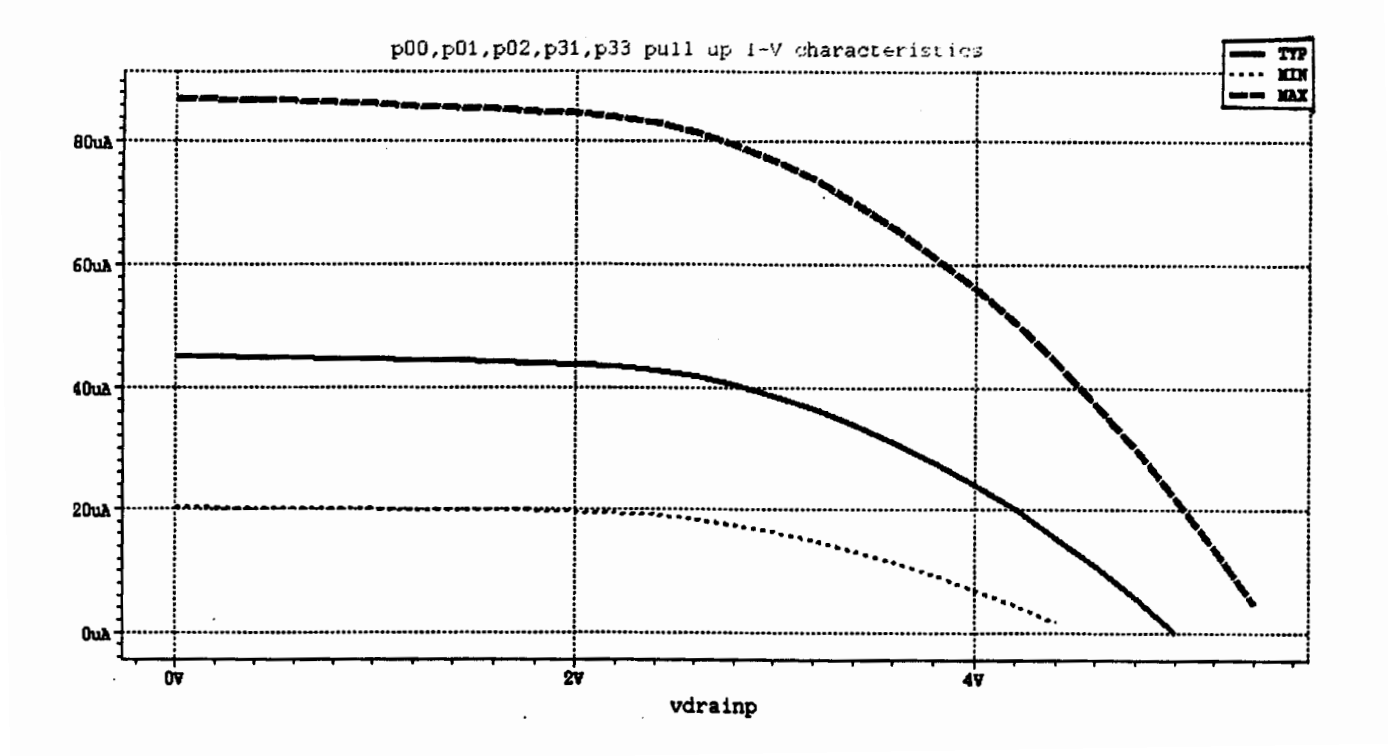


Figure 8. Current vs Pin Voltage Values

PIN FUNCTIONS (Continued)

Port 2 (P27-P20). Port 2 is an 8-bit, bit programmable, bi-directional, CMOS-compatible I/O port. These eight I/O lines can be configured under software control to be input or output, independently. Bits programmed as outputs may be globally programmed as either push-pull or open-drain. When configured as inputs, P20 and P22 have 10 kOhm (typical) pull-up resistors (Figure 9). However, P21 and P23 do not have resistors (Figure 10).

When configured as inputs, P24-P27 are configured with a voltage divider. The voltage divider consists of an internal 25K pull-up resistor (Figure 11), and a 7.5K pull-down resistor. The input levels on P24-P27 are adjusted for connection to the emitters of the opto-transistors and switch at a voltage level of 0.4 V_{DD} (± 300 mV). For input voltages on P24-P27, refer to Table 3.

Table 3. P24-P27 Input Open Circuit Voltage (No off-chip resistance)

V_{DD}	Min	Max
4.5V	0.95V	1.15V
5.0V	1.05V	1.25V
5.5V	1.15V	1.39V

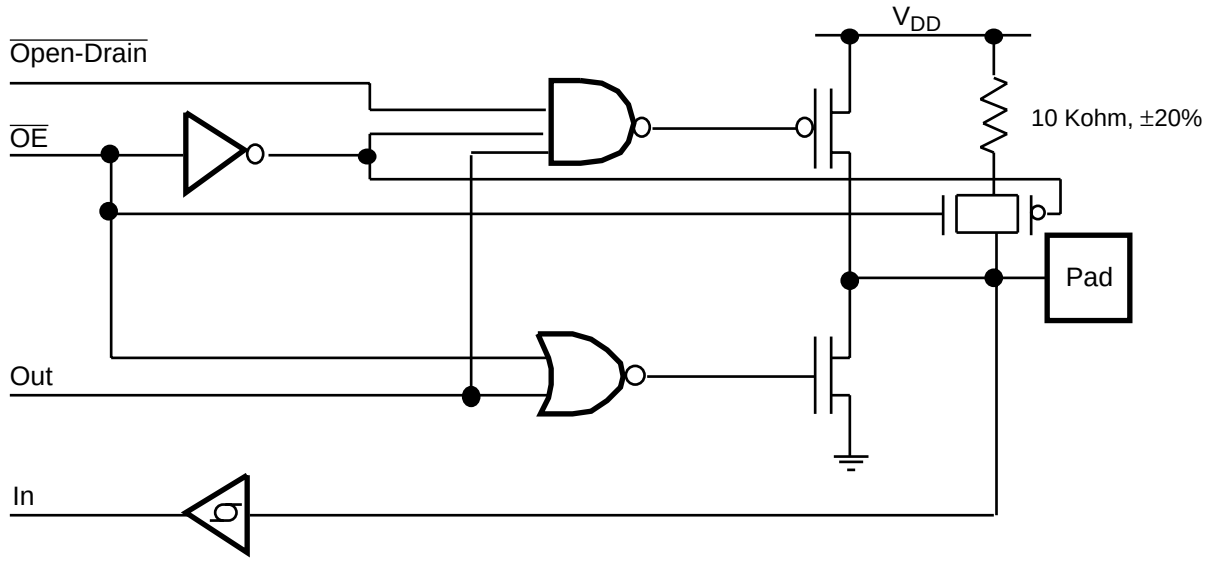


Figure 9. Port 2 P20, P22 Configuration

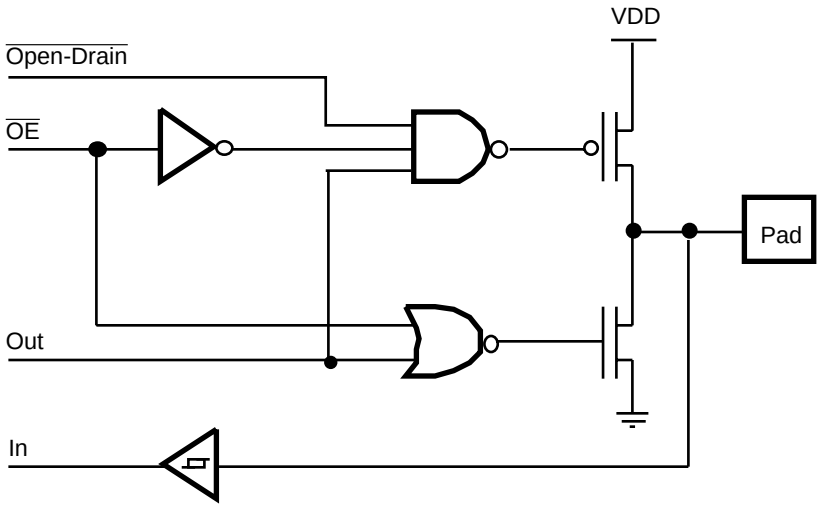


Figure 10. Port 2 P21, P23 Configuration

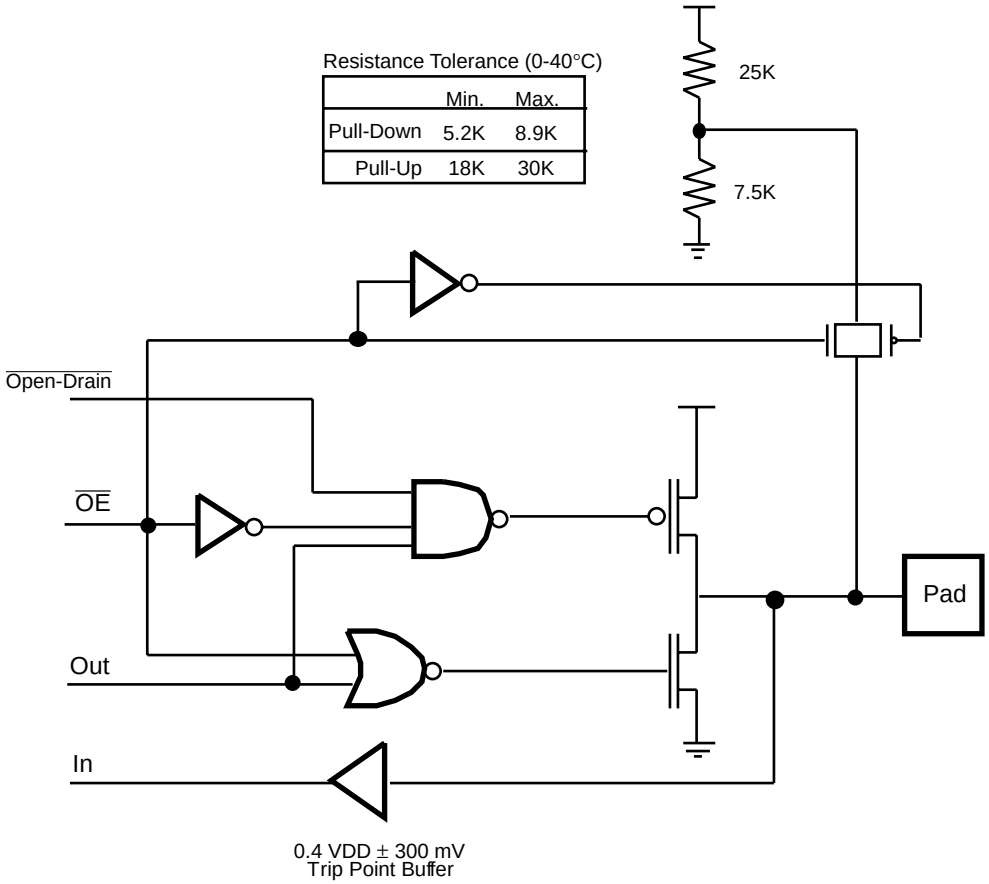


Figure 11. Port 2 P27-P24 Configuration

PIN FUNCTIONS (Continued)

Port 3 (P33, P31). Port 3 is a 2-bit, CMOS-compatible port with two fixed input lines (P33, P31). These two lines can also be used as the interrupt sources IRQ2 and IRQ1. P31 can also be configured as a timer input. Both lines can be configured through ROM mask selection to sink or source current emulating a 100K pull-up or pull-down resistor (Figure 12). Port 33-31 can be accessed through the P3 register. The upper 4 bits of this 8-bit register always reads "1111." Bit D2 reads 0 and Bit D0 reads 1. Bits D3 and D1 represent P33 and P31 respectively (see Figure 36).

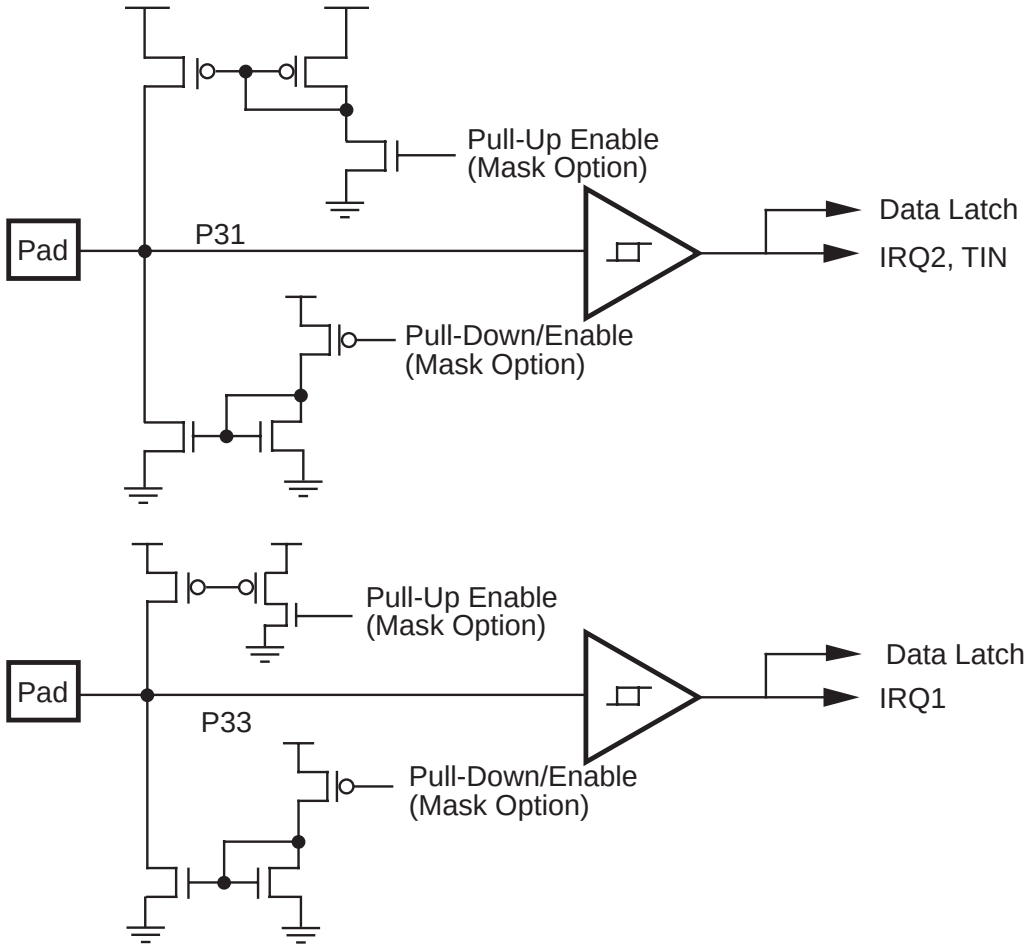


Figure 12. Port 3 P33, P31 Configuration

FUNCTIONAL DESCRIPTION

The Z86319 MCU incorporates the following special features to enhance the Z8 architectural core for use in mice, trackballs, and other consumer applications.

Reset. Upon power-up, the Power-On Reset circuit waits for TPOR, plus 18 clock cycles, then starts program execution at address 000CH (Figure 13). The Z86319 control registers' reset values are shown in Table 4.

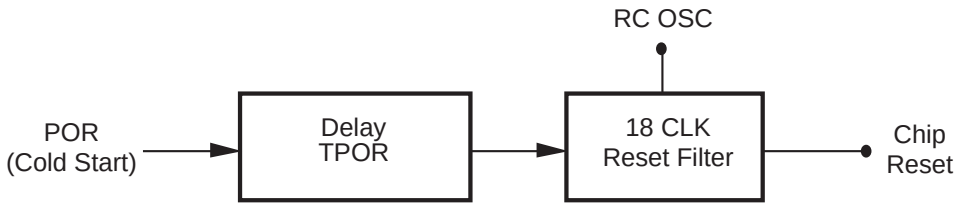


Figure 13. Internal Reset Configuration

Table 4. Z86319 Control Registers

		Reset Values								
Addr.	**Reg.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Comments**
F1	TMR	0	0	0	0	0	0	0	0	
F2	T1	U	U	U	U	U	U	U	U	
F3	PRE1	U	U	U	U	U	U	0	0	
F4	T0	U	U	U	U	U	U	U	U	
F5	PRE0	U	U	U	U	U	U	U	0	
F6	P2M	1	1	1	1	1	1	1	1	Inputs after reset
F7	P3M	U	U	U	U	U	U	1	0	
F8	P01M	U	U	U	0	U	U	0	1	
F9	IPR	U	U	U	U	U	U	U	U	
FA	IRQ	U	U	0	0	0	0	0	0	
FB	IMR	0	U	U	U	U	U	U	U	
FC	FLAGS	U	U	U	U	U	U	U	U	
FD	RP	U	U	U	U	U	U	U	U	
FF	SPL	U	U	U	U	U	U	U	U	

FUNCTIONAL DESCRIPTION (Continued)

Program Memory. The Z86319 can address up to 2 KB of internal program memory (Figure 14). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain four 16-bit vectors that correspond to the four available interrupts. Bytes 0-2047 are on-chip mask-programmed ROM.

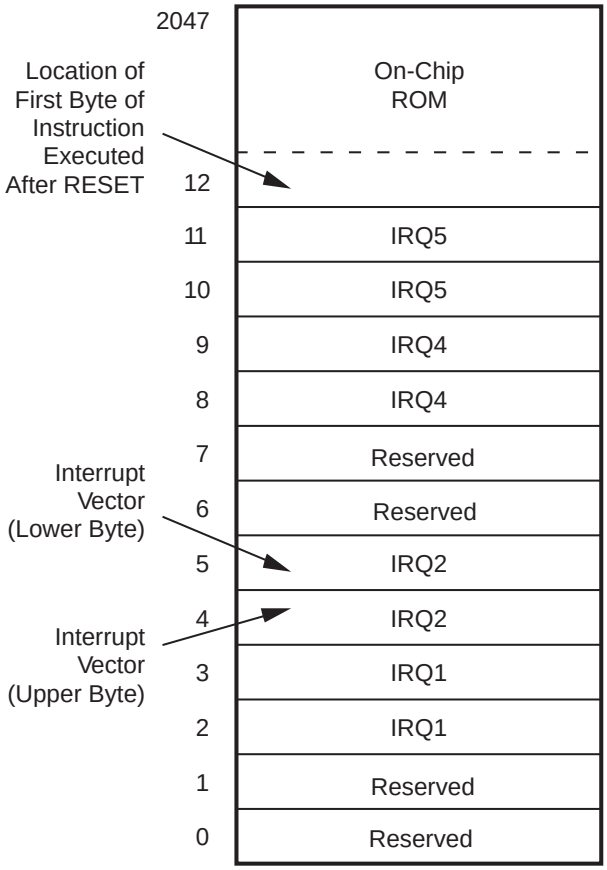


Figure 14. Program Memory Map

Register File. The Register File consists of three I/O port registers, 125 general-purpose registers, and 14 control and status registers, R0-R3, R4-R127 and R241-R255, respectively (Figure 15). The Z86319 instructions can access registers directly or indirectly via an 8-bit address field. This field allows short, 4-bit register addressing using the Register Pointer. In the 4-bit mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

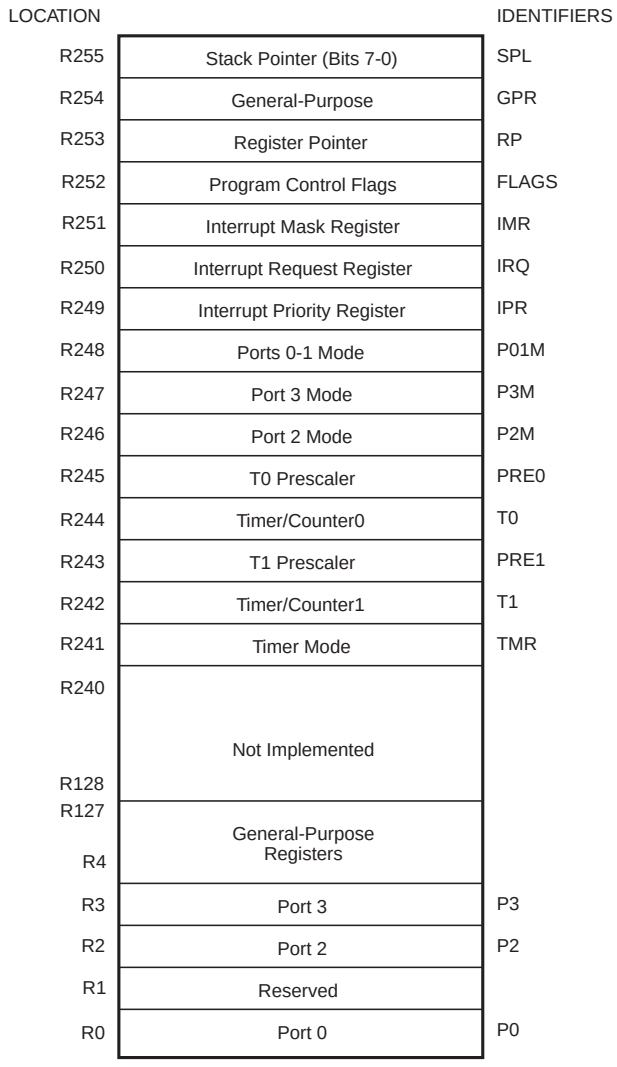


Figure 15. Register File

Stack Pointer. The Z86319 features an 8-bit Stack Pointer (R255) used for the internal stack that resides within the general-purpose registers.

Counter/Timer. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler can be driven by internal or external clock sources, however, the T0 can be driven by the internal clock source only (Figure 16).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1) is generated.

The counter can be programmed to start, stop, continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input via Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or not retriggerable, or as a gate input for the internal clock.

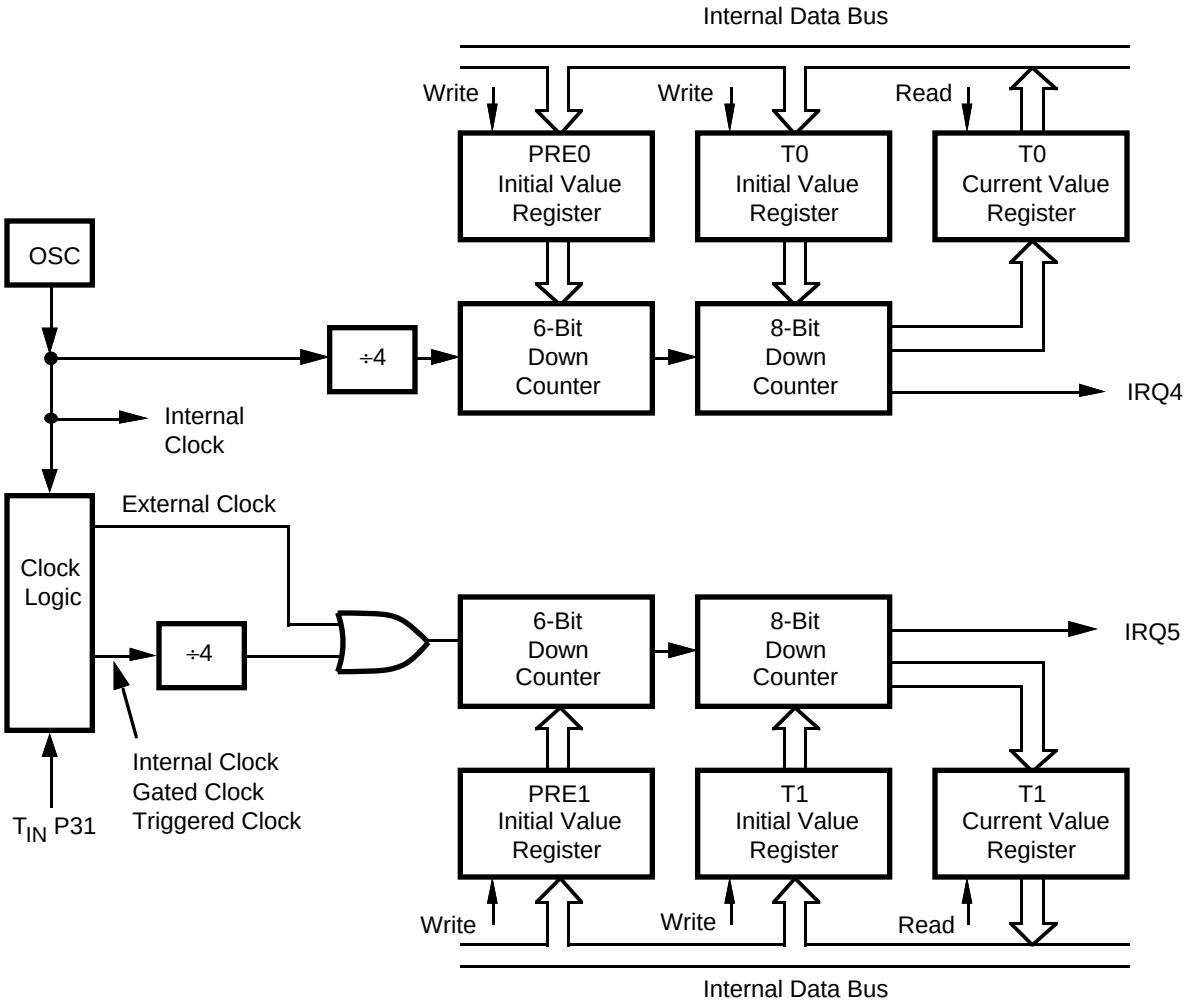


Figure 16. Counter/Timers Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z86319 features four interrupts from four different sources. These interrupts are maskable and prioritized (Figure 17). The four sources are divided as follows: the falling edge of P31, P33, and the two counter/timers. The Interrupt Mask Register globally or individually enables or disables the four interrupt requests (Table 5).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z86319 interrupts are vectored through locations in program memory. When an interrupt machine cycle is activated, an interrupt request is granted, thereby disabling all subsequent interrupts, saving the Program Counter and Status Flags, and branching to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the Interrupt Service Routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request Register is polled to determine which of the interrupt requests requires service.

Table 5. Interrupt Types, Sources, and Vectors

Source	Name	Vector	Location	Comments
P33	IRQ1	2,3	External	Falling Edge
P31	IRQ2	4,5	External	Falling Edge
T0	IRQ4	8,9	Internal	
T1	IRQ5	10,11	Internal	

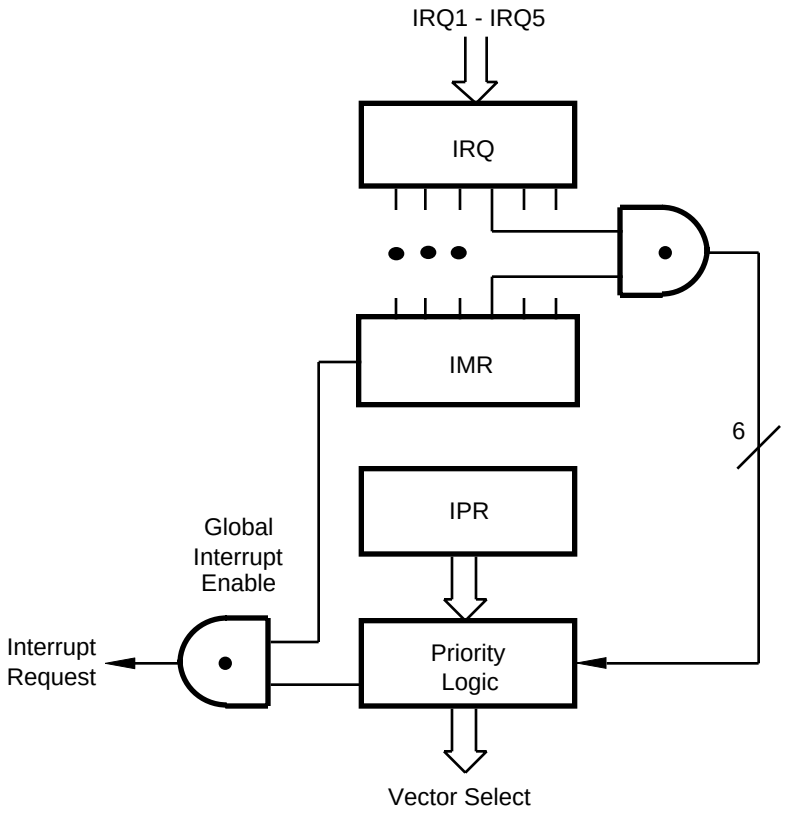


Figure 17. Interrupt Block Diagram

RC Oscillator. The Z86319 features an on-chip RC precision oscillator that requires a 1% precision resistor externally connected between V_{DD} and pin 6 (Figure 18). The tolerance of the RC oscillator is less than ±10% over the voltage range of 4.5V to 5.5V and over a temperature range of 0-40°C. Pin 7 is the Analog Ground for the oscillator.

Increased parasitic board capacitance will slow down the RC oscillator and deteriorate the RC frequency tolerance. The minimum and maximum parasitic board capacitances are 0.5 pF and 2 pF, respectively.

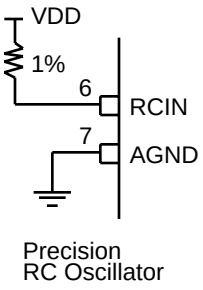


Figure 18. Oscillator Configuration

HALT Mode. This instruction turns off the internal CPU clock but not the precision RC oscillator. The counter/timers, their interrupts, and external interrupts IRQ1 and IRQ2 remain active. The device can be recovered by interrupts, either externally or internally generated. An interrupt must be enabled prior to the HALT Mode, and executed to exit the HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT.

In order to enter HALT Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To flush the pipeline, the user must execute a NOP (Opcode=FFH) immediately before the HALT instruction. i.e.:

```
FF      NOP     ; clear the pipeline
7F      HALT    ; enter the HALT Mode
```

In HALT Mode, the value of each output line prior to the HALT instruction is retained.

Watch-Dog Timer (WDT). The Watch-Dog Timer is enabled upon power-up of the MCU and is clocked by its own internal RC oscillator. The WDT instruction does not affect the Zero (Z), Sign (S), and Overflow (V) flags.

Opcode WDT (5FH). Execution of WDT clears the WDT counter. The time interval between any 2 consecutive WDT instructions has to be smaller than T_{WDT} min.

Low Voltage Protection (V_{LV}). The device will function normally between 5.5V and 4.5V under all specified conditions. Below 4.5V, the device is still internally functional until the Low Voltage trip point (V_{LV}) is reached, however, it is not guaranteed to meet all AC and DC Characteristics. When the supply voltage drops below V_{LV}, an automatic hardware reset occurs as V_{DD} returns above V_{LV}. Essentially, this action helps in reinitializing the Z86319.

The actual V_{LV} is a function of temperature, operating frequency and process parameters. The typical V_{LV} is a function of the ambient temperature for a frequency of 4 MHz. The device is functional down to V_{LV} voltage. The min. operational V_{DD} is determined by the value of the V_{LV} voltage at ambient temperatures. The V_{LV} voltage increases as the temperature decreases (Figure 19).

FUNCTIONAL DESCRIPTION (Continued)

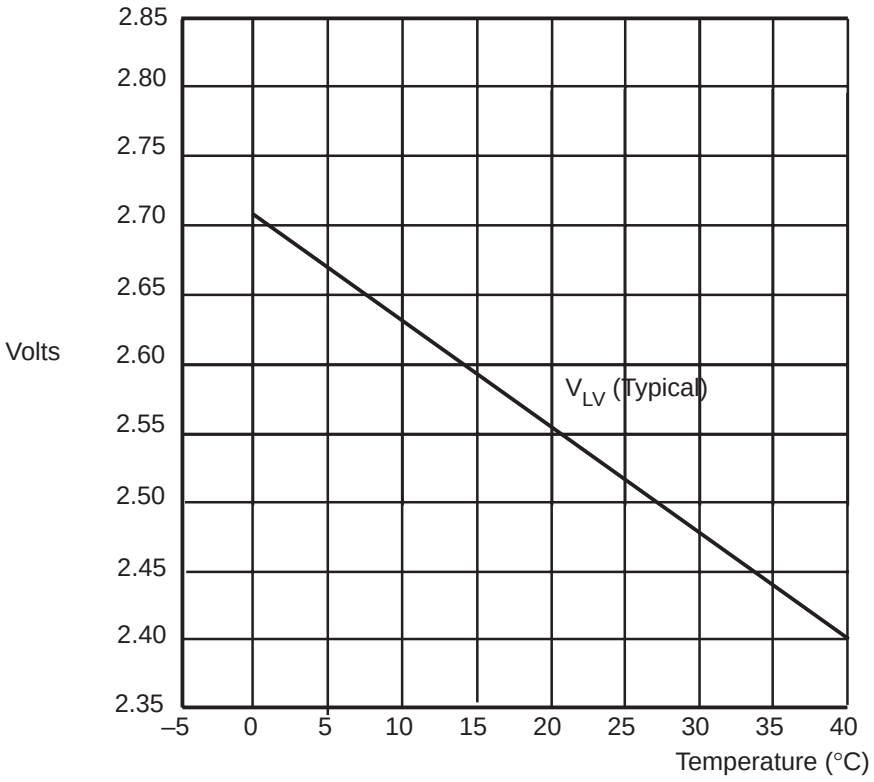


Figure 19. Typical Z86319 VLV vs Temperature

Z8 CONTROL REGISTERS

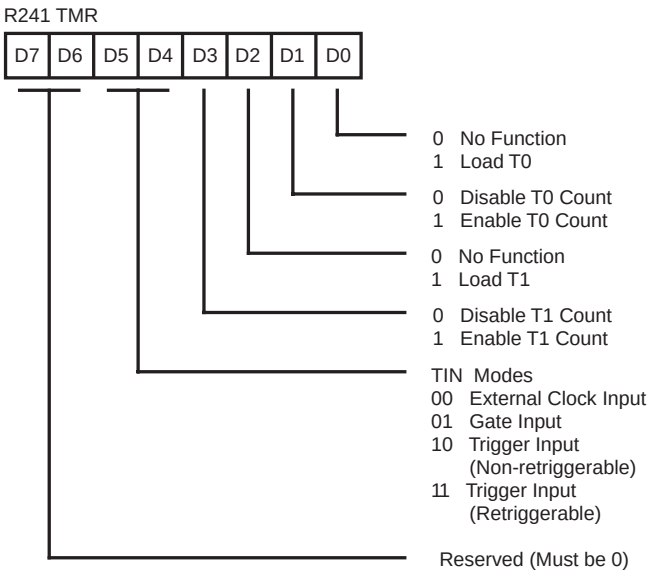


Figure 20. Timer Mode Register (F1H: Read/Write)

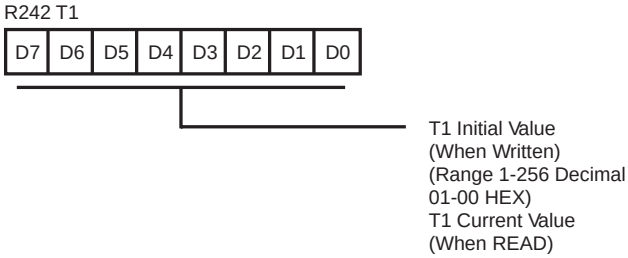


Figure 21. Counter Timer 1 Register (F2H: Read/Write)

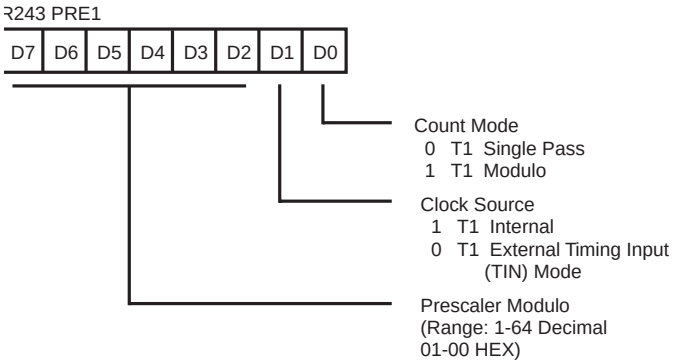


Figure 22. Prescaler 1 Register (F3H: Write Only)

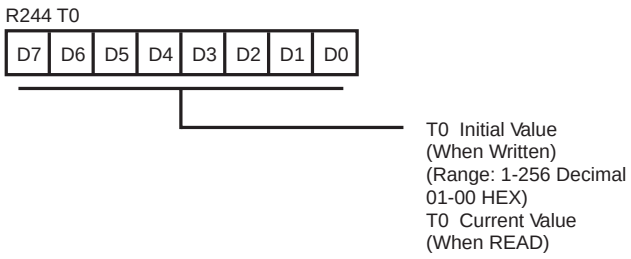


Figure 23. Counter/Timer 0 Register (F4H: Read/Write)

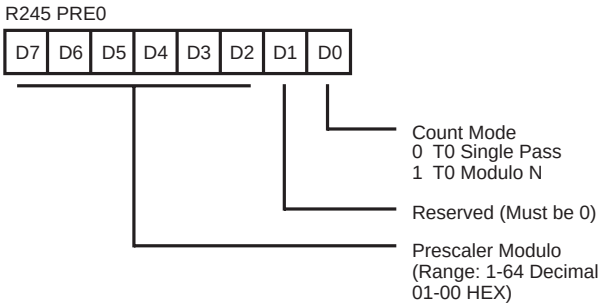


Figure 24. Prescaler 0 Register (F5H: Write Only)

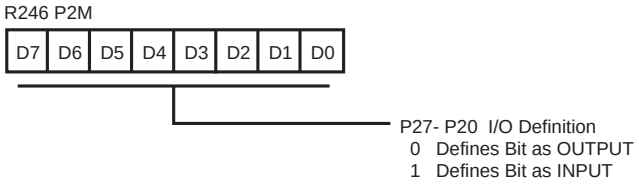


Figure 25. Port 2 Mode Register (F6H: Write Only)

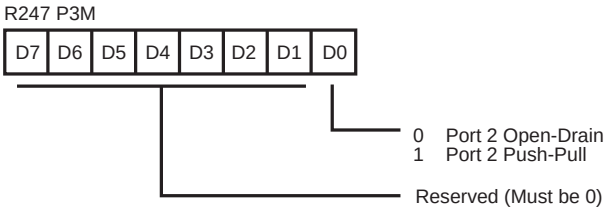


Figure 26. Port 3 Mode Register (F7H: Write Only)

Z8 CONTROL REGISTERS (Continued)

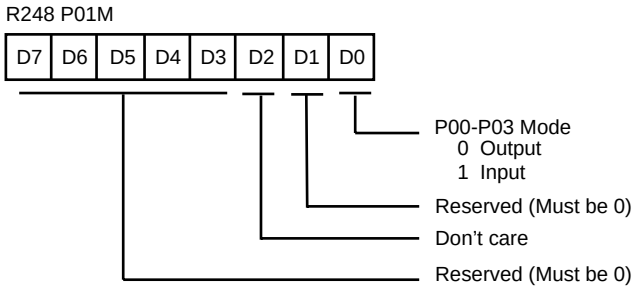


Figure 27. Port 0 and 1 Mode Register (F8H: Write Only)

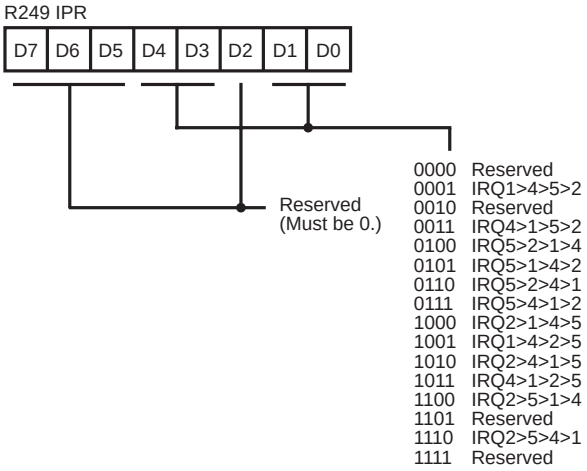


Figure 28. Interrupt Priority Register (F9H: Write Only)

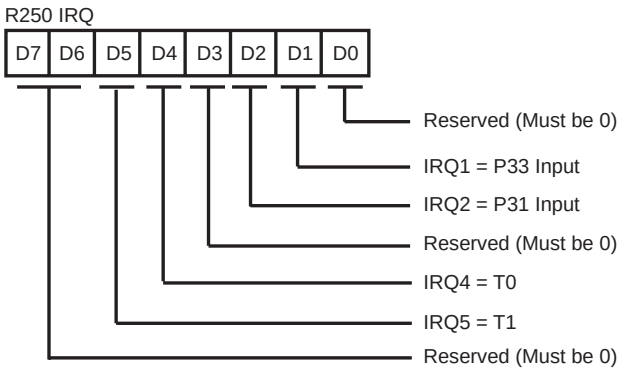

R250 IRQ
D7 D6 D5 D4 D3 D2 D1 D0
Reserved (Must be 0)
IRQ1 = P33 Input
IRQ2 = P31 Input
Reserved (Must be 0)
IRQ4 = T0
IRQ5 = T1
Reserved (Must be 0)

Figure 29. Interrupt Request Register (FAH: Read/Write)

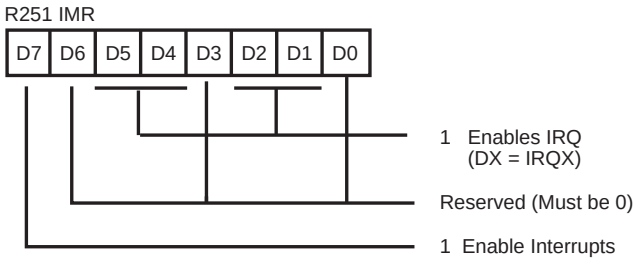


Figure 30. Interrupt Mask Register (FBH: Read/Write)

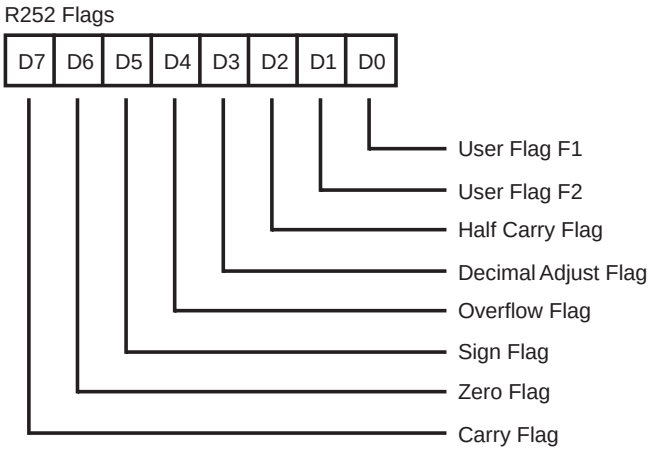


Figure 31. Flag Register (FCH: Read/Write)

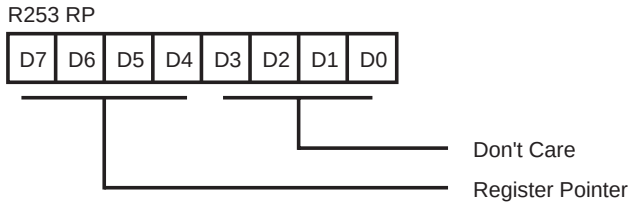


Figure 32. Register Pointer (FDH: Read/Write)

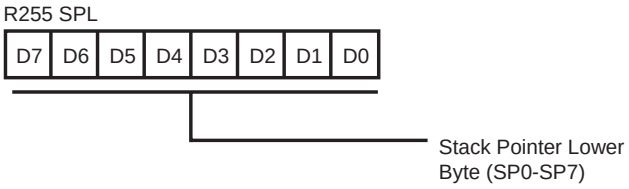


Figure 33. Stack Pointer (FFH: Read/Write)

Z8 PORT REGISTERS

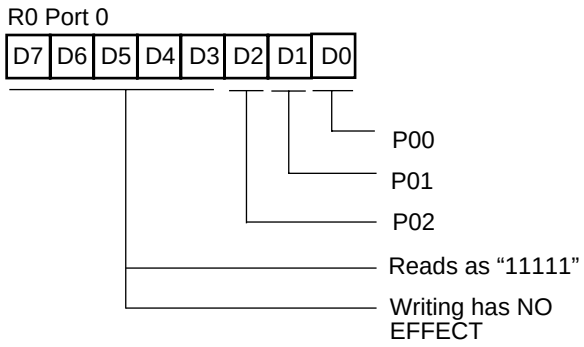


Figure 34. Port 0 Register (Read/Write)

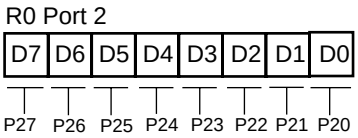


Figure 35. Port 2 Register (Read/Write)

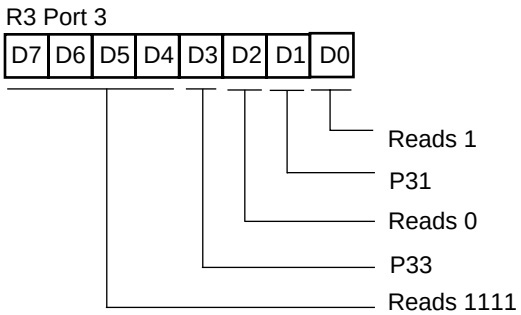
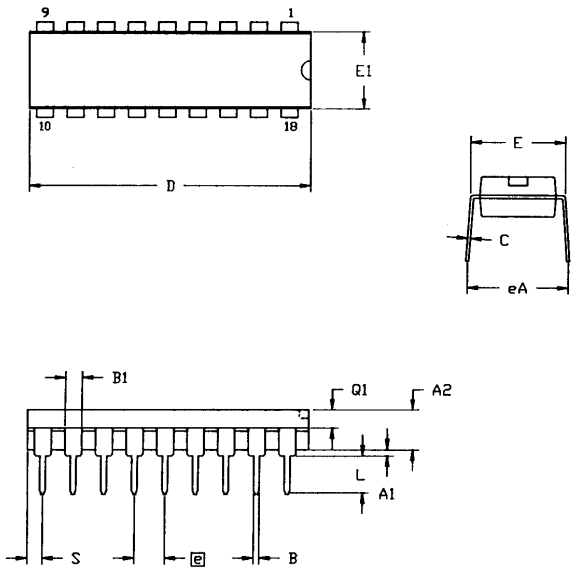


Figure 36. Port 3 Register (Read Only)

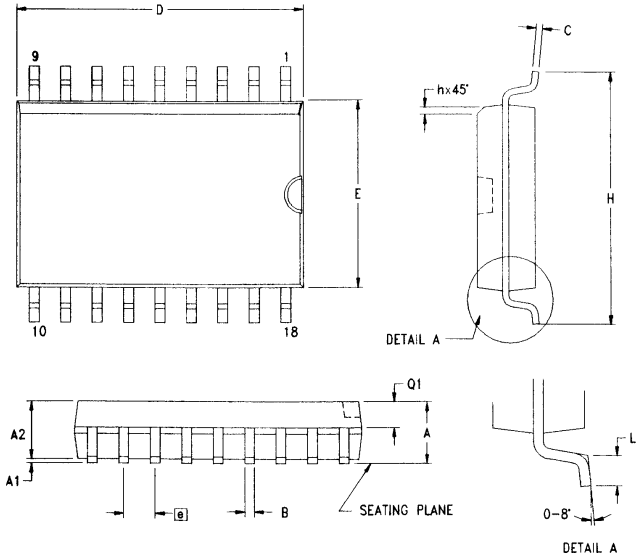
PACKAGING INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

Figure 37. 18-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	0.094	0.104
A1	0.10	0.30	0.004	0.012
A2	2.24	2.44	0.088	0.096
B	0.36	0.46	0.014	0.018
C	0.23	0.30	0.009	0.012
D	11.40	11.75	0.449	0.463
E	7.40	7.60	0.291	0.299
e	1.27 TYP		0.050 TYP	
H	10.00	10.65	0.394	0.419
h	0.30	0.50	0.012	0.020
L	0.60	1.00	0.024	0.039
Q1	0.97	1.07	0.038	0.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 38. 18-Pin SOIC Package Diagram

ORDERING INFORMATION

Z86319

Z8631904PSC Z8631904SSC

For fast results, contact your local Zilog sales offices for assistance in ordering the part required.

CODES

Package
P = DIP
S = SOIC

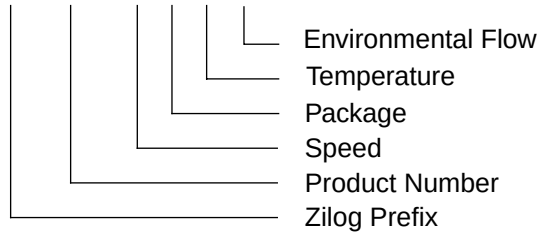
Temperature
S = 0°C to +40°C

Speed
04 = 4 MHz

Environmental
C = Plastic Standard

Example:

Z 86319 0 4 P S C is a Z86319, 4 MHz, DIP, 0° to +40°C, Plastic Standard Flow



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